REMARKS

Claims 3-8 and 10-13 are pending in this application. By this Amendment, claims 1, 2 and 9 were cancelled. New claims 11-13 were added. The rejections set forth in the Office Action are respectfully traversed below.

Rejections Under 35 U.S.C. §112, first paragraph:

Claims 1 - 9 were rejected under 35 U.S.C. §112, first paragraph, basically for features recited in claim 1. These rejections are now moot since claims 1, 2 and 9 were cancelled and claims 3 - 8 now depend from claim 10 (also amended). Therefore, these rejections should be withdrawn.

Rejections Under 35 U.S.C. §102(b):

Claims 1, 3 and 9 were rejected under 35 U.S.C. §102(b) over each of **Shimakura, Lucas et al.**, and **Imaizumi et al.**, respectively. These rejections are now moot since claims 1 and 9 were canceled and claim 3 now depends from claim 10.

Rejections Under 35 U.S.C. §103(a):

Claims 3, 4 and 10 were rejected under 35 U.S.C. §103(a) over the Admitted Prior Art ("APA") in view of **Imaizumi et al.** Claims 5 - 8 were rejected under 35 U.S.C. §103(a) over the APA in view of **Imaizumi et al.** and in further view of **Kirchner et al.**

Amended claim 10 recites a TiO_2 layer. When the TiO_2 layer is not provided in the structure

of claim 10, Ti atoms in the gate electrode inevitably cause diffusion into the compound semiconductor layer, resulting in a large variation of threshold voltage as represented in Fig. 2, even in the case the penetrating depth of the Ti atoms is small. It should be noted that the relationship of Fig. 2 was discovered by the inventor in the investigation constituting the foundation of the present invention. By providing the TiO_2 layer as set forth in amended claim 10, the threshold variation is suppressed successfully as represented in Fig. 6.

The Examiner contends that the subject matter of claim10 is derived from the combination of Fig. 1 of the present application labeled as Related Art and **Imaizumi**. However, it should first be noted that Fig. 1 is labeled as Related Art and not Prior Art. Thus, relying on Fig. 1 as Prior Art in order to establish these rejections is not proper.

Nevertheless, even if the structure of Fig. 1 could be regarded as Prior Art, the subject matter of claim 10 is not derived from the combination with **Imaizumi**, as **Imaizumi** merely addresses the subject matter of increasing the gate breakdown voltage and minimizing the reverse leakage current by increasing the Schottky barrier eight of the gate electrode. There is no suggestion at all to suppress the threshold voltage change caused by diffusion of Ti atoms. Thus, there is no motivation for a person skilled in the art to apply the teaching of **Imaizumi** to the structure of Fig. 1.

Furthermore, note that **Lucas**, teaching the anti-reflective coating, is silent about specific combination of TiO_2 layer with the gate electrode having the stacked structure of Ti/Pt/Au as set forth in amended claim 10. In view of different object of the invention, there is no motivation for a person skilled in the art to modify the teaching of **Lucas** to derive the subject matter of claim 10.

Thus, it is submitted that claim 10, and also the claims dependent from claim 10, are distinct from any of the cited references either alone or in combination.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

John P. Kong
Attorney for Applicant
Reg. No. 40,054

JPK/kal
Atty. Docket No. **001701**
Suite 1000, 1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/746,064

3. (Amended) A compound semiconductor [triode] field effect transistor as claimed in claim [1] 10, wherein said [insulating metal oxide] TiO_2 layer has a stoichiometric composition.

4. (Amended) A compound semiconductor [triode] field effect transistor as claimed in claim [1] 10, wherein said [insulating metal oxide film] TiO_2 layer has a non-stoichiometric composition.

5. (Amended) A compound semiconductor [triode] field effect transistor as claimed in claim [1] 10, wherein said compound semiconductor device further includes first and second ohmic electrodes in contact with said compound semiconductor layer at both lateral sides of said gate electrode, and wherein [insulating metal oxide film] TiO_2 layer is provided further at an interface between said first ohmic electrode and said compound semiconductor layer and between said second ohmic electrode and said compound semiconductor layer.

6. (Amended) A compound semiconductor [triode] field effect transistor as claimed in claim 5, wherein said [insulating metal oxide film] TiO_2 layer has a thickness allowing tunneling of carriers therethrough.

7. (Amended) A compound semiconductor [triode] field effect transistor as claimed in claim [1] 6 wherein said [metal oxide film] TiO_2 layer is provided so as to cover a surface of said compound semiconductor layer continuously from said first ohmic electrode to said gate

electrode and from said gate electrode to said second ohmic electrode.

8. (Amended) A semiconductor triode as claimed in claim [1] 10, wherein said channel layer includes a two-dimensional electron gas.

10. (Amended) A compound semiconductor [device] field effect transistor, comprising:

a compound semiconductor layer including a channel [region] layer;

a gate electrode electrically contacting said compound semiconductor layer to control a current flow in said channel layer, said gate electrode having a multi-layer structure including a Ti layer, a Pt layer and an Au layer; and

an intermediate layer including a TiO_2 layer, formed [provided] between said Ti layer and said compound semiconductor layer.